Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listings of Claims:

1. (original) A nonvolatile semiconductor memory comprising a memory array which includes a plurality of nonvolatile memory elements which store data in terms of threshold voltage levels, said memory being adapted to implement:

a first operation of applying a first voltage which corresponds to an unselection state at data reading, to plural word lines in said memory array and detecting a current flow through any of the memory elements on the word lines, thereby finding the presence of a failing element in said memory array; and

a second operation, which is implemented upon finding the presence of a failing memory element by said first operation, of applying said first voltage to one of said plural word lines, while applying a second voltage, which is lower than said first voltage, to remaining word lines and detecting a current flow through any nonvolatile memory

element, thereby pinpointing a failing memory element having a threshold voltage lower than a prescribed voltage level.

2. (original) A nonvolatile semiconductor memory according to claim 1, wherein said first and second operations are initiated in response to entry of control signals and address signals from the outside, and a result of detection of said second operation is released to the outside.

3. (original) A nonvolatile semiconductor memory comprising a memory array which includes a plurality of nonvolatile memory elements which store data in terms of threshold voltage levels, said memory being adapted to implement:

a first operation of applying a first voltage which corresponds to an unselection state at data reading, to plural word lines in said memory array and detecting a current flow through any of the memory elements on the word lines, thereby finding the presence of a failing element in said memory array;

a second operation, which is implemented upon finding the presence of a failing memory element by said first operation, of applying said first voltage to one of said plural word lines, while applying a second voltage, which is lower than said first voltage, to remaining word lines and detecting a current flow through a nonvolatile memory element coupled to any of said word lines, thereby pinpointing a failing memory element having a threshold voltage lower than a prescribed voltage level; and

a third operation of raising the threshold voltage of said failing memory element having the lower threshold voltage on said one word line by use of data which is held in a read-out amplifier by said second operation.

4. (original) A nonvolatile semiconductor memory according to claim 3, wherein said memory array comprises a plurality of first memory element sets each including a plurality of nonvolatile memory elements coupled in parallel to a first bit line or a first source line.

5. (original) A nonvolatile semiconductor memory according to claim 4, wherein said memory array comprises a plurality of second memory element sets each including a

plurality of said first memory element sets, said first operation being implemented for each of said second memory element sets at a time.

6. (original) A nonvolatile semiconductor memory according to claim 5 including a plurality of said memory arrays, said first and second operations being implemented concurrently for said plural memory arrays.

7. (original) A nonvolatile semiconductor memory according to claim 6, wherein said first operation is or said first, second and third operations are implemented at the time of power-on.

8. (original) A nonvolatile semiconductor memory according to claim 6, wherein said nonvolatile memory elements have their threshold voltage shifted up by a writing operation and shifted down by an erasing operation, and

wherein said first operation or said first, second and third operations are implemented at the time of power-on following a power supply cutoff during the erasing operation.

9. (original) A storage device comprising:

a nonvolatile semiconductor memory including a memory array which includes a plurality of nonvolatile memory elements which store data in terms of threshold voltage levels, said memory being adapted to implement:

a first operation of applying a first voltage which corresponds to an unselection state at data reading, to plural word lines in said memory array and detecting a current flow through any of the memory elements on the word lines, thereby finding the presence of a failing element in said memory array; and

a second operation of applying said first voltage to one of said word lines, while applying a second voltage, which is lower than said first voltage, to remaining word lines and detecting a current flow through any nonvolatile memory element, thereby pinpointing a failing memory element having a threshold voltage lower than a prescribed voltage level,

and adapted to release results of finding and detection of said first and second operations to the outside; and

a control circuit which is adapted to issue control signals and address signals for initiating said first and second operations to said nonvolatile semiconductor memory,

said control circuit issuing a first control signal and a first address signal for initiating said first operation to said nonvolatile semiconductor memory, issuing to said nonvolatile semiconductor memory, depending on the result of finding of said first operation, a second control signal and a second address signal for initiating said second operation, and issuing to said nonvolatile semiconductor memory, depending on the result of detection of said second operation, a third control signal and a third address signal for initiating a third operation which raises the threshold voltage of the nonvolatile memory element having the lower threshold voltage than the prescribed voltage level detected by said second operation.

10. (original) A storage device according to claim 9, wherein said memory array comprises a plurality of first memory element sets each including a plurality of nonvolatile memory elements coupled in parallel to a bit line or a source line.

Claim 11 (canceled).